34

Vertical
Addressing
Circuit

40

ROW
DRIVERS

30

PIXEL ARRAY

42

READOUT, GAIN & ADC

DIGITAL
SIGNALS

TIMING
AND
CONTROL

Horizontal
Addressing
Circuit

44

32

FIG. 1

ARRAY 30

49A 49B 49M 49N

50		50	...	50		50	...	50
50		50		50		50	
50		50		50		50	

AMPLIFICATION
AND
ANALOG-TO-DIGITAL
CONVERSION
CIRCUITRY
52

AMPLIFICATION
AND
ANALOG-TO-DIGITAL
CONVERSION
CIRCUITRY
52

54

DIGITAL
SIGNALS

FIG. 2

FROM COLUMN 49A

S/H 60A

62A (+)

gain select

X 66

S/H 68

Vref2 Vref3

CALIBRATION NETWORK 72

Vref1

(+) 70

ADC 74

76

S

FROM COLUMN 49B

S/H 60B

62B (+)

Vref4

64

analog mux

52

select from column decoder

FIG. 3

FIG. 4

Pixel Output

V_{signal} V_{reset}

Input to amplification stage

V_{cl} $(V_{reset} - V_{signal})$

Photogate for selected row

RST for selected row

Switch SS   closed

Switch S1   closed

SAMPLE AND HOLD TIMING

FIG. 5

90

out

VCC

VCC

M110

M112

M120

M118

M120

M120

V_0

drain+

M115

VCC

M111

M132

V-

M131

M130

V+

M8

0

Bias Current

Bias Current

FIG. 6

G(Vrsl-Vsig)

Op amp offset

Op amp output

Vcl

Switch S10 — closed

Switch S15 — closed

Switch S14 — closed

Switch S8 — closed — closed
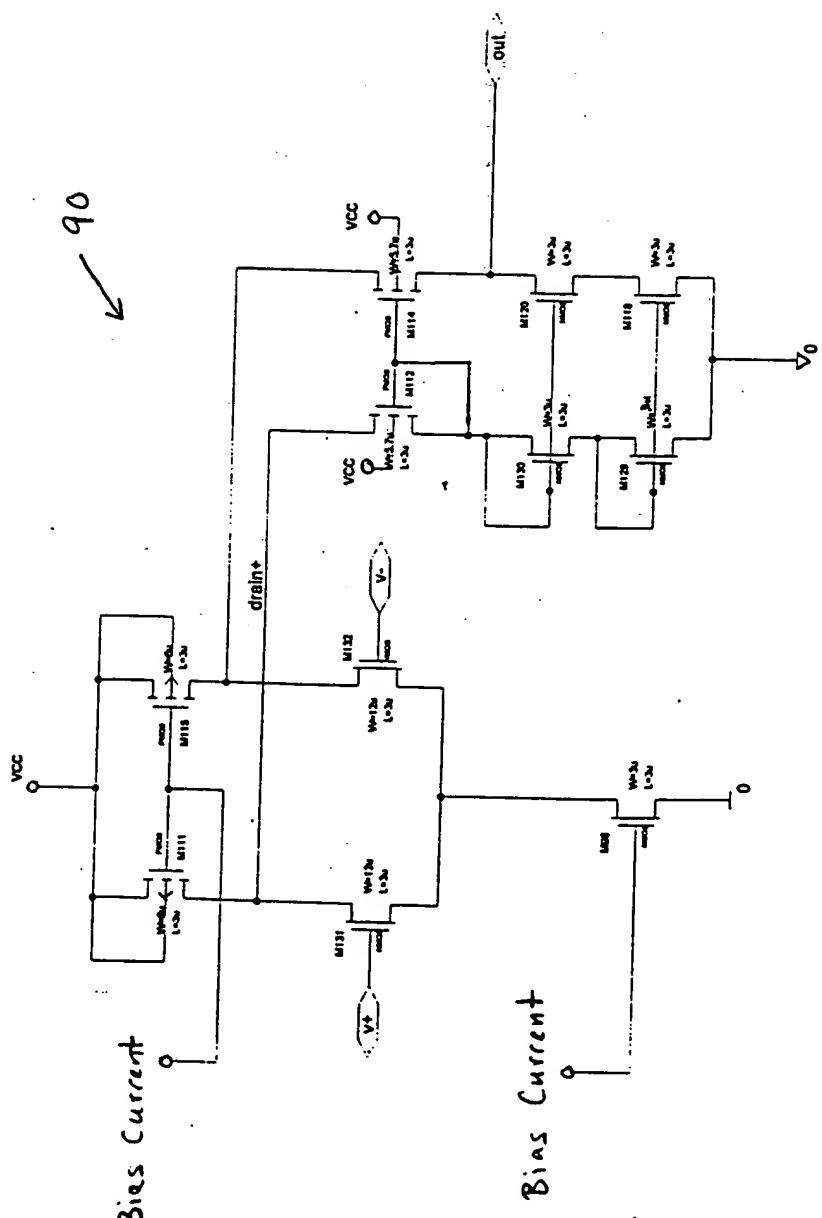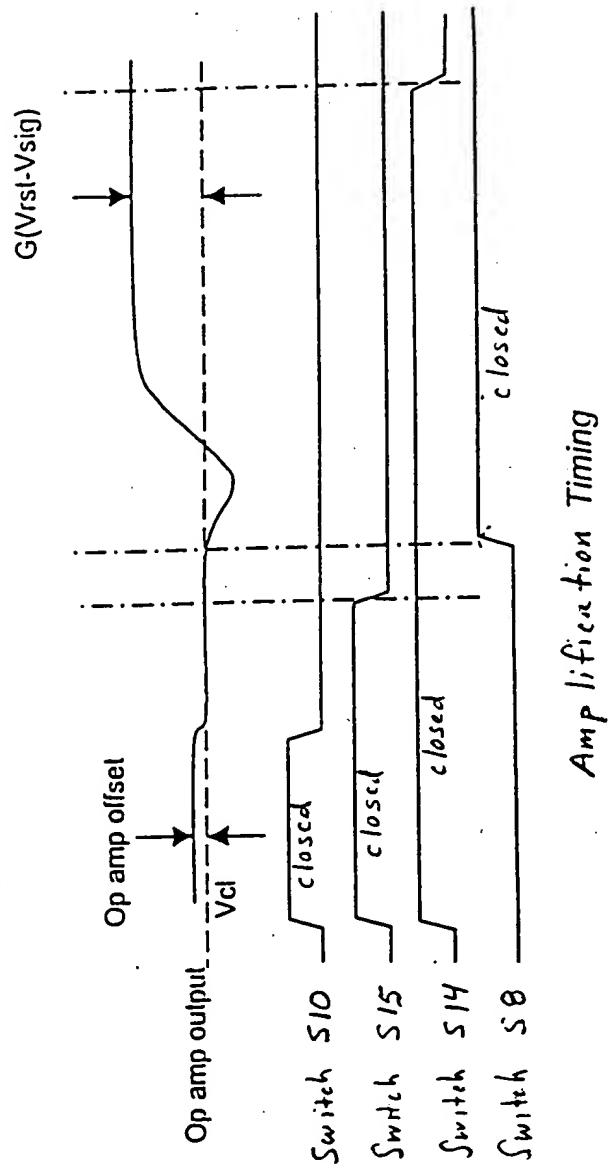
Amplification Timing

FIG. 7

FIG. 8

Comparison results:

Comparison results:

0 MSB → 0 → 1 → 1 → 1 → 1 → 0 → 1 → 1 LSBs

$Vcl + C\ (VREF1 - Vclamp1)$ ----

$Vcl + \dfrac{C}{2}\ (VREF1 - Vclamp1)$ ----

$Vcl + \dfrac{C}{4}\ (VREF1 - Vclamp1)$ ----

Vcl ----

$Vcl + G\ (V_{reset} - V_{signal})$

$FIG.\ 9$

FIG. 10

Switch S14 (at output of op amp 90)

closed

clear

pre2bar

preset-bar (for MSB)

preset-bar (for LSB)

strobe (to comparator 92)

select (for MSB)

select (for LSB)

transfer-enable

enable-offset
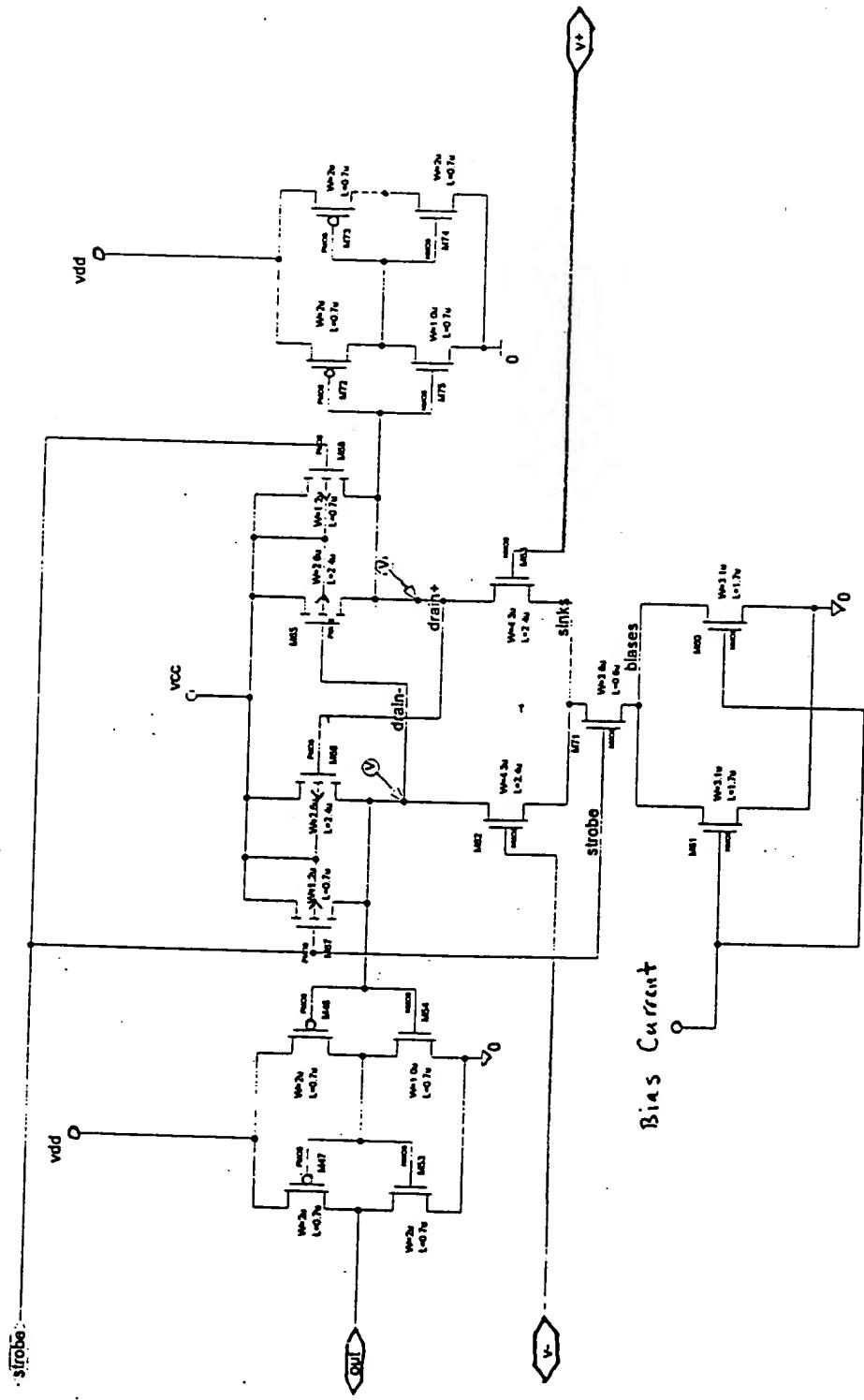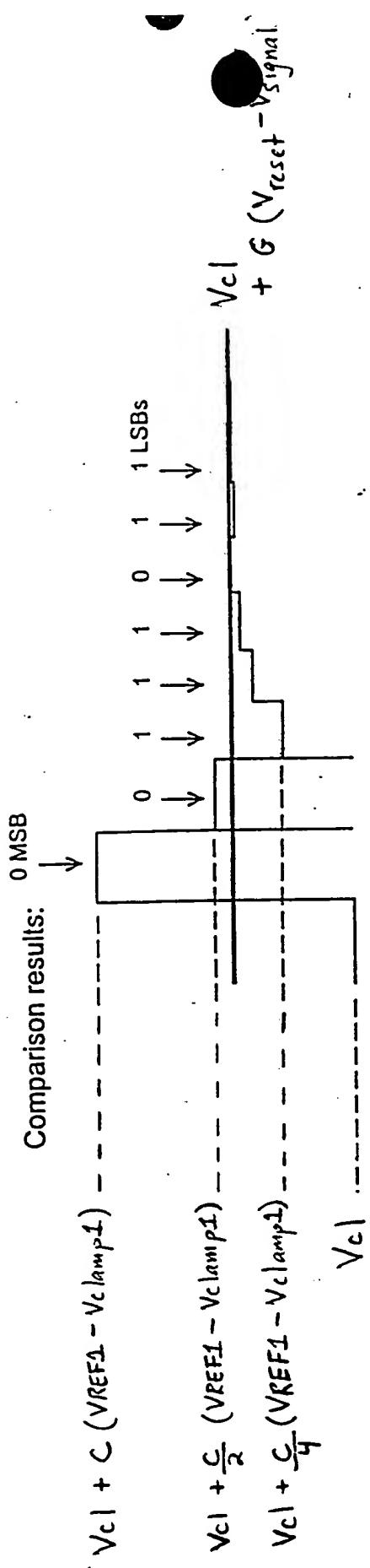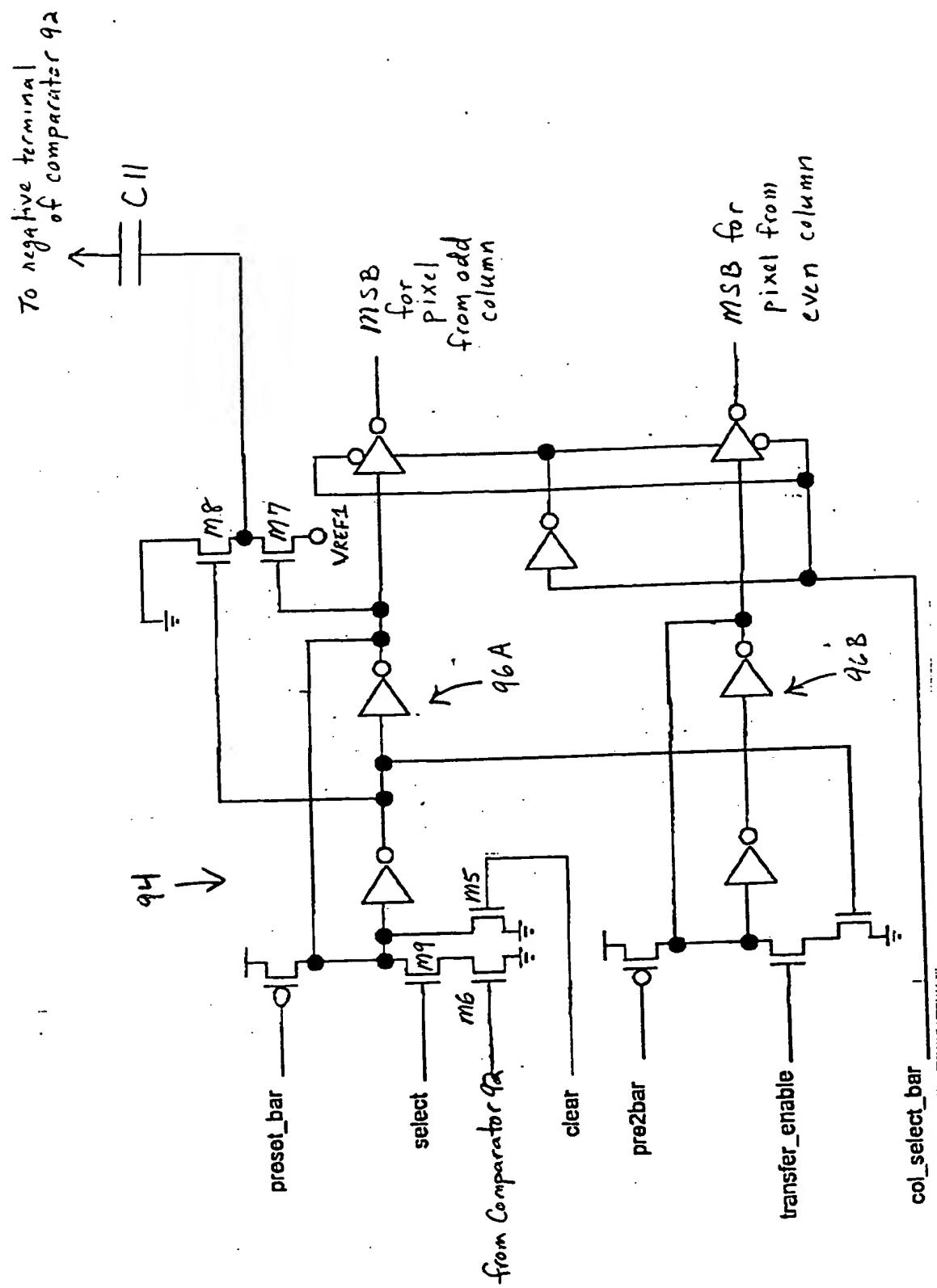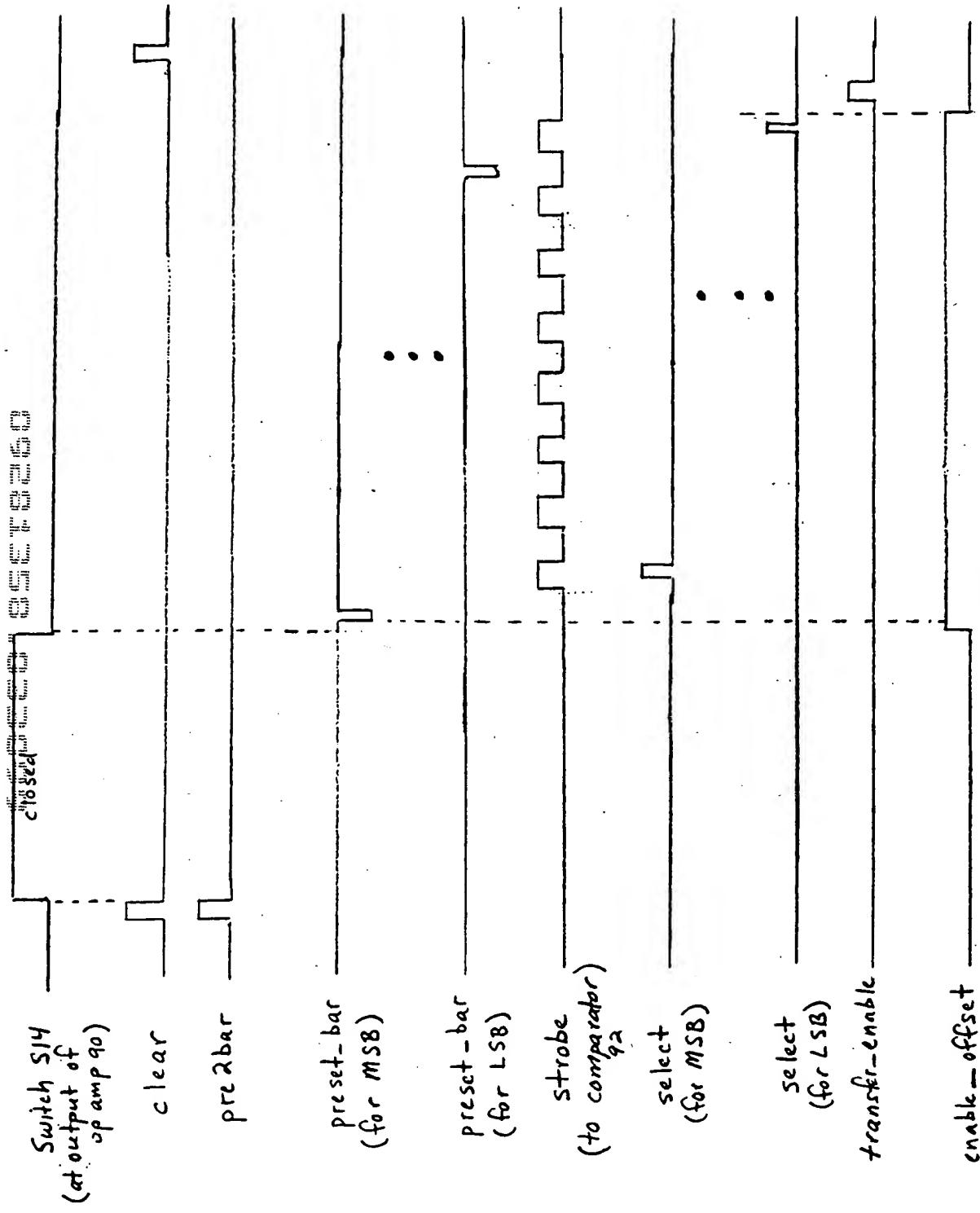
AMPLIFICATION

ANALOG-TO-DIGITAL CONVERSION

FIG. 11

to negative terminal of comparator 9a

C19

M13

M11

M12

M15

Vref2

102

"clamp_data"

M14

M10

M17

M16

100

enable_offset

cpreset_bar

cselect

from comparator 9a

cclr

FIG. 12

cclr

Clamping Switch S15   closed

Network Clamping Switch S16   closed

enable offset

cpreset — bar
(for MSB)

cpreset — bar
(for LSB)

strobe
(to comparator
9a)

cselect
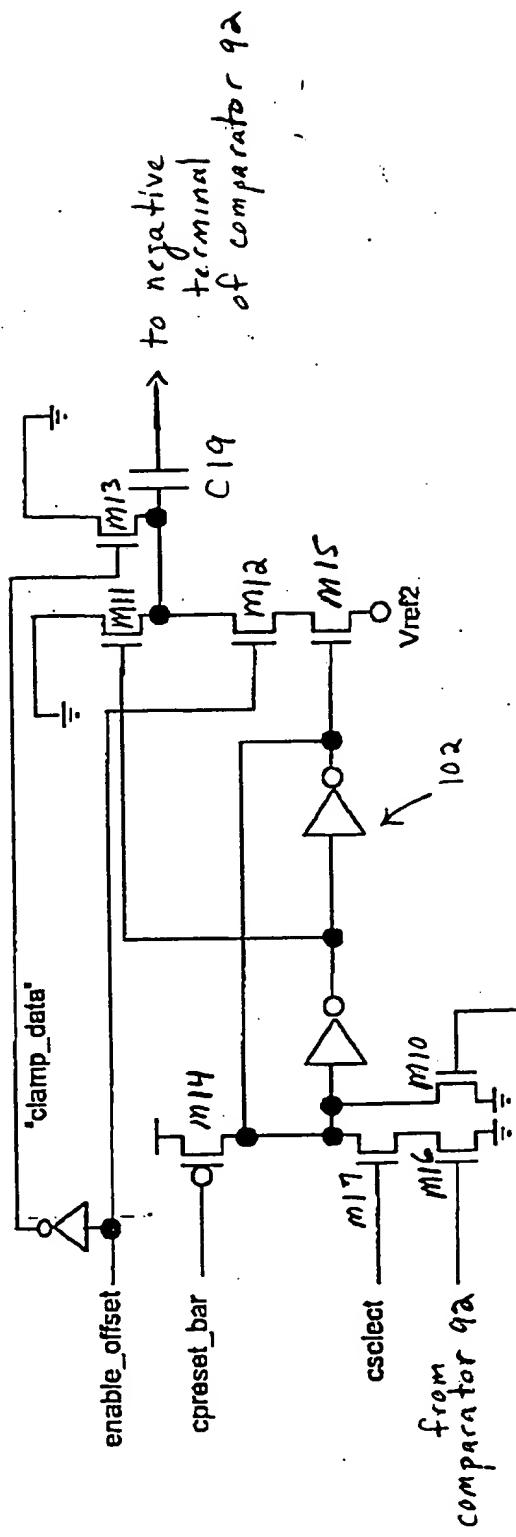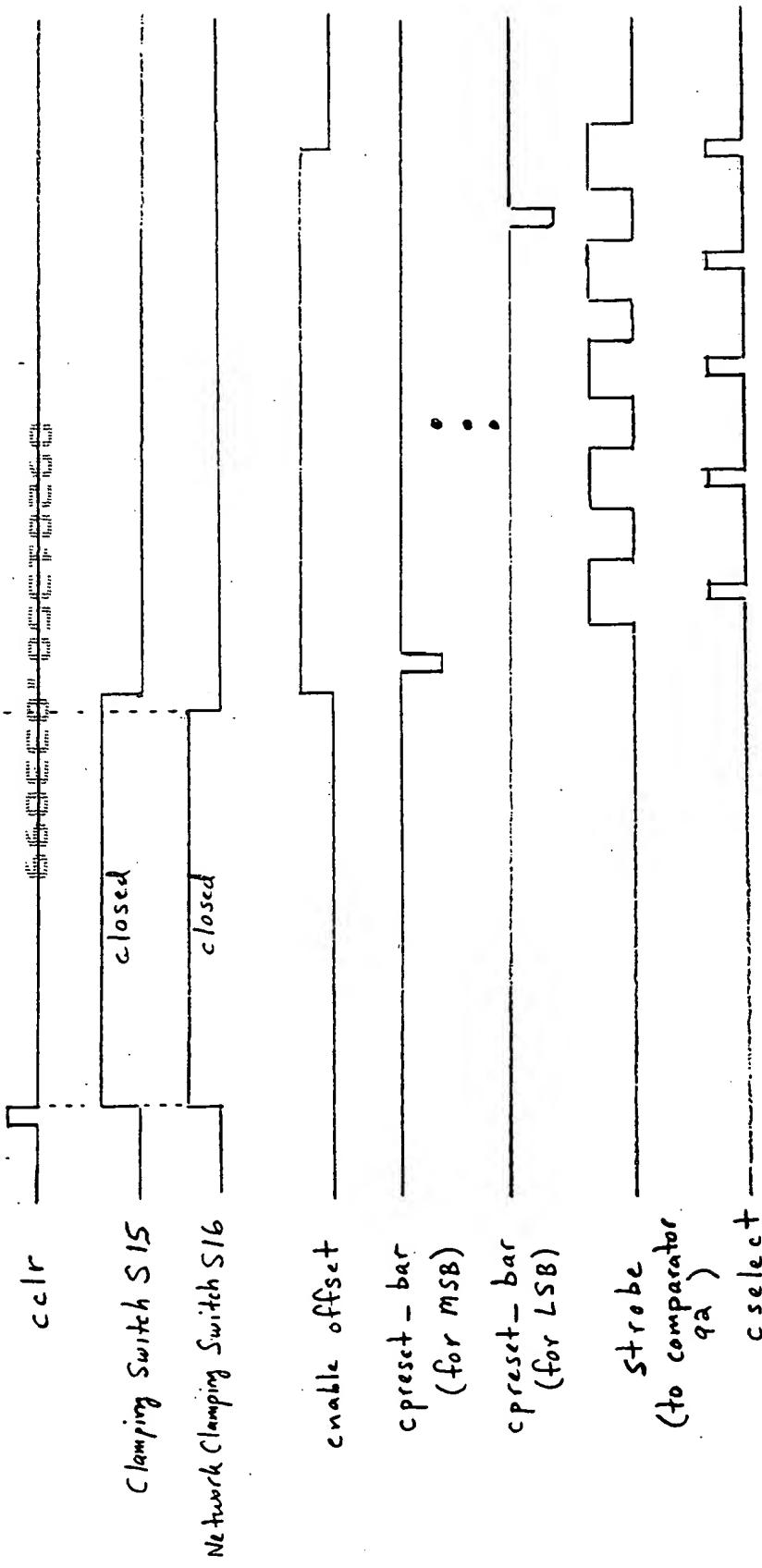
CALIBRATION TIMING

FIG. 13

Fig 14

pixel timing

RST

shs

shr

node_reset

FIG. 15

gain timing

node_reset

CL2

phi_out

phi_rst

phi_r0

phi_s0

VCL

op amp output

op amp input
α+
source-follower side of gain
capacitors C35 through C39

$G \times (V_{reset} - V_{signal})$

$(V_{reset} - V_{signal})$

$FIG. 16$

1700

1702

RS

1708

1706

RS

(another
pixel)

1710

1718

FIG17

CONTROLLER — 1810

pixel column
line output

ADC   1800   ADC   ADC

8 bit output
bus for
readout

• • •   1802

storage for:
byte #1
byte #2
byte #3
...
byte #n

18   1804
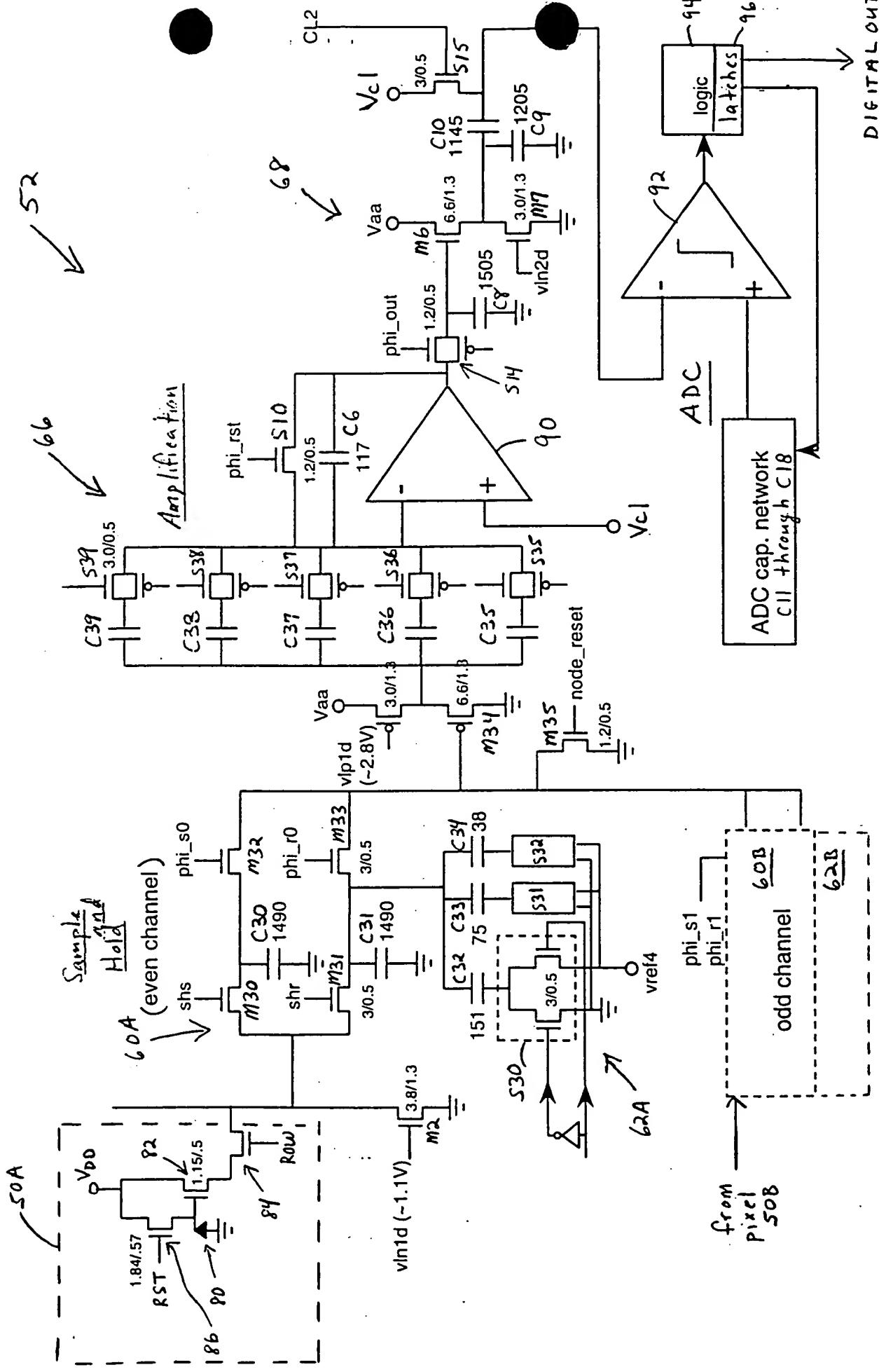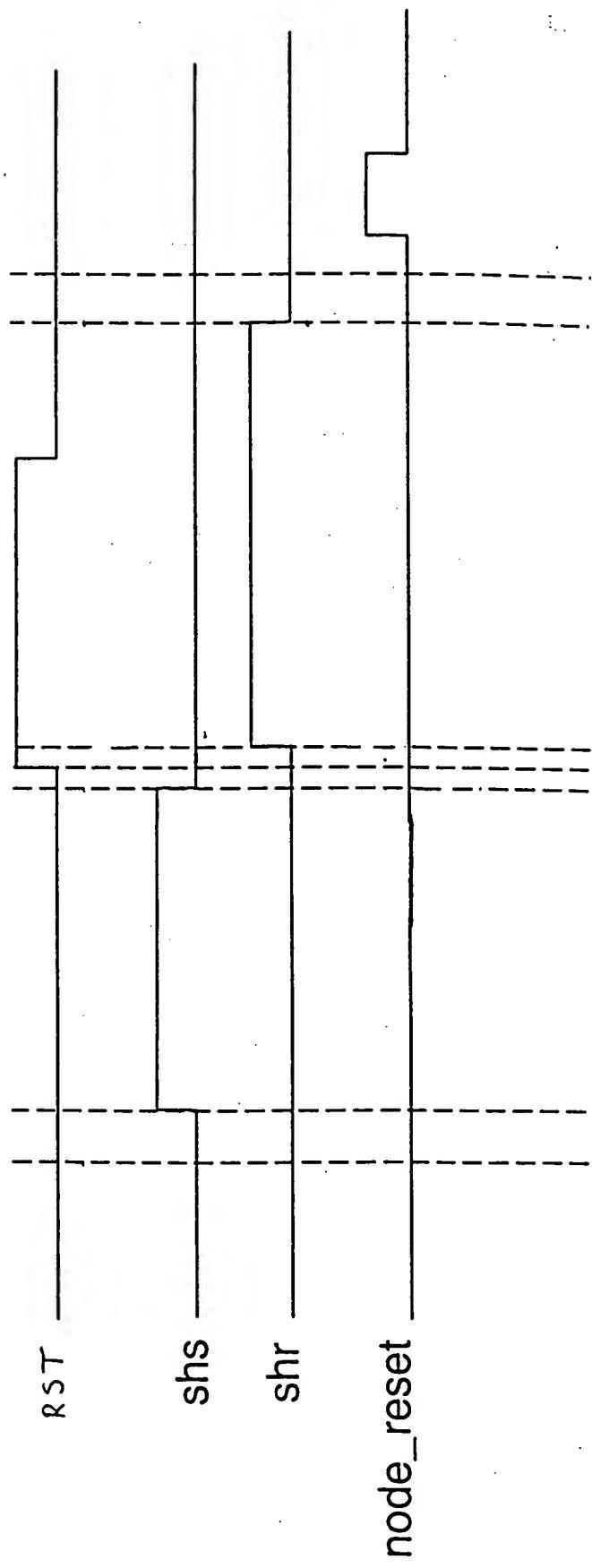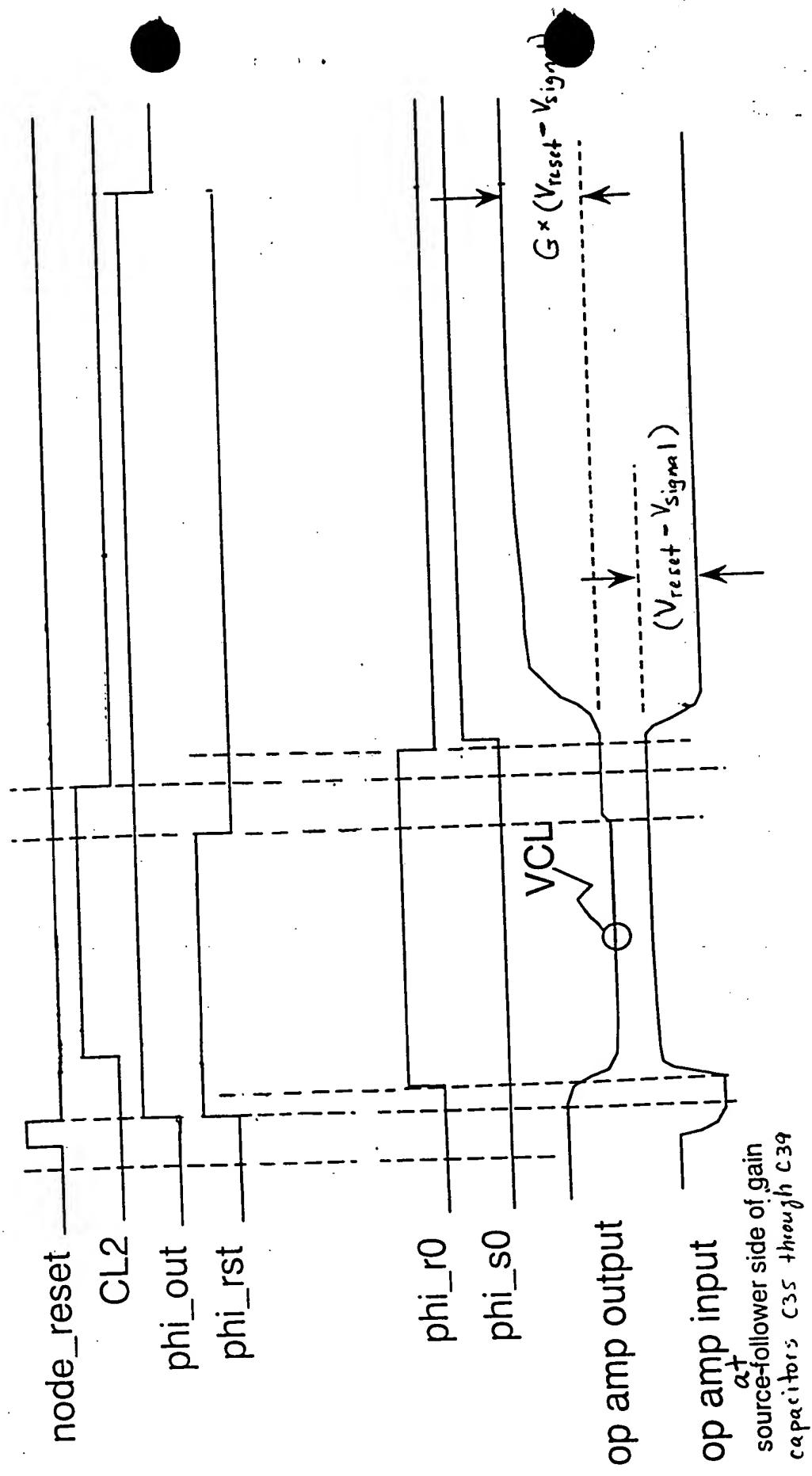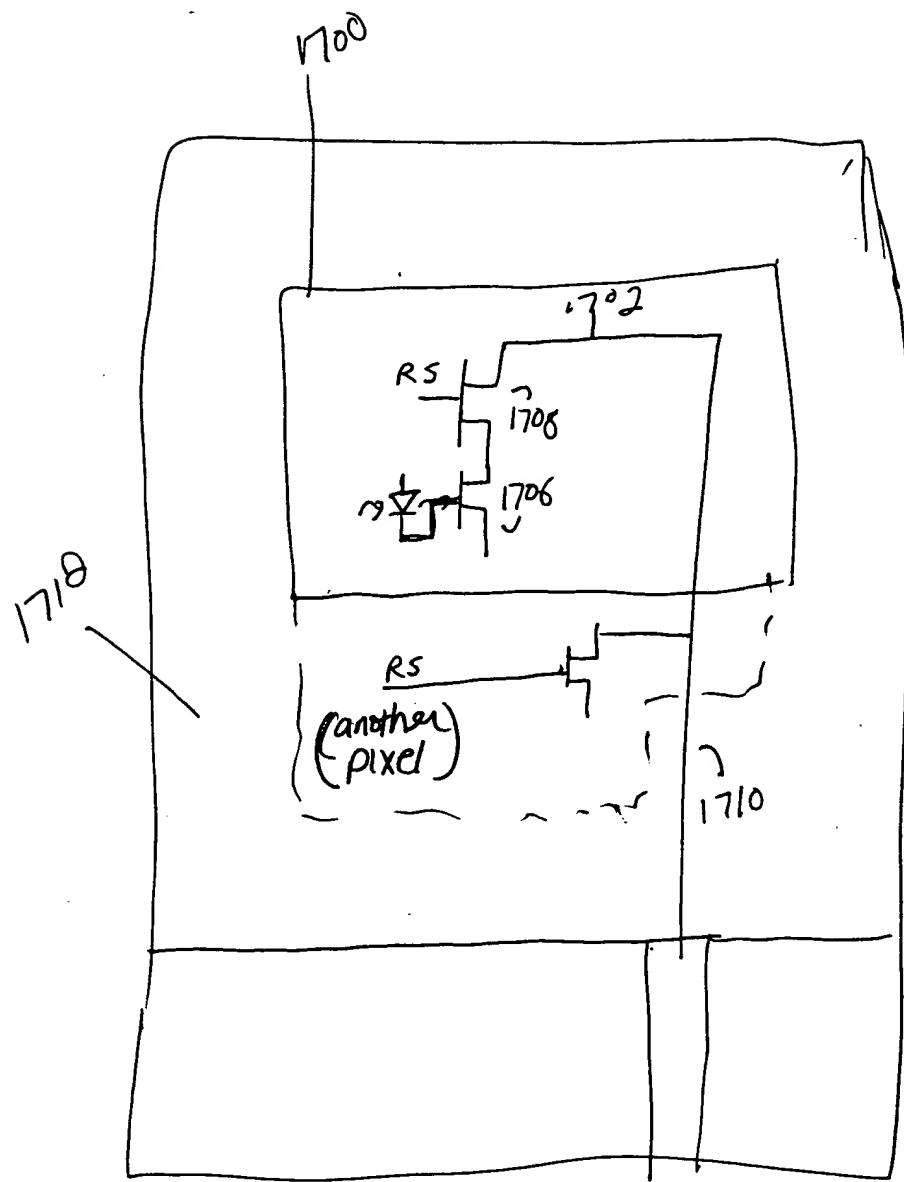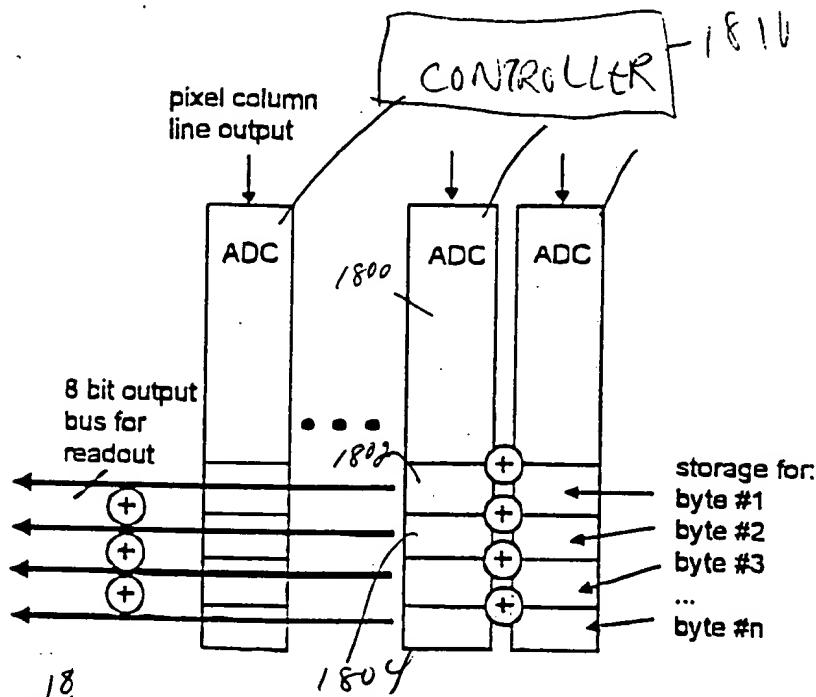
Figure 1. Multiple byte storage inside ADC for column wise multiplexing of the ADC. Arithmetic processing of neighbors also shown.

2 Byte Storage ADC
3/30/98 R. Panicacci